EE 434 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _
Exam 2
Fall 2006

Instructions. Students may bring 2 pages of notes to this exam. There are 10 questions and 5 problems. The questions are worth 2 points each and the problems are all worth 16 points. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If references semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda = 0$, and $\gamma = 0$. If reference to a bipolar process is made, assume this process has key process parameters $J_S=10^{-15}A/\mu^2$, $\beta=100$ and $V_{AF}=\infty$. If any other process parameters are needed,use the process paramaters associated with the process described on the last page of this exam. Specify clearly what process parameters you are using in any solution requiring process parameters.

1. The fan-in capacitance of a minimum-sized equal rise/fall CMOS inverter in a process where $\mu_n/\mu_p=3$ and $V_{TN}=-V_{TP}$ is $4C_{OX}W_{MIN}L_{MIN}$. What is the fan-in capacitance of a minimum-sized inverter in the same process?

2. Four types of power dissipation in digital circuits were discussed. Which of these four is dominant in process with feature sizes at the 65nm level and smaller?

3. A minimum-sized BJT is typically much larger than a minimum-sized MOSFET if comparable processing equipment is used. What process step in the bipolar process is the major contributor to this much larger size?

4. True or False - The dynamic power dissipation of a pad driver designed to drive a 10pF load is significantly less than that required to drive the 10pF load directly with a minimum-sized inverter.

5. How does the total propagation delay ($T_{HL}+T_{LH}$) for an inverter sized for equal rise and fall times (with minimum-sized n-channel devices) compare to that of an inverter with minimum-sized devices if they both drive a load of 20fF?

6. How does the total propagation delay ($T_{HL}+T_{LH}$) for an inverter sized for equal rise and fall times (with minimum-sized n-channel devices) compare to that of an inverter with minimum-sized devices if the equal rise/fall inverter drives an identical equal rise/fall inverter and if the minimum-sized inverter drives an identical minimum-sized inveerter?

6. From a dynamic power dissipation viewpoint, are Boolean implementations with multiple-input NAND gates or multiple-input NOR gates preferred? Why?

7. In a MOSFET, describe the difference in shape of the inversion layer when the device is operating in deep triode compared to that when the device is operating in saturation.

8. What power is required in the last inverter of a pad driver to take a 1GHz clock signal off-chip if it is driving a 4pF load with V_H=5V and V_L=0V?

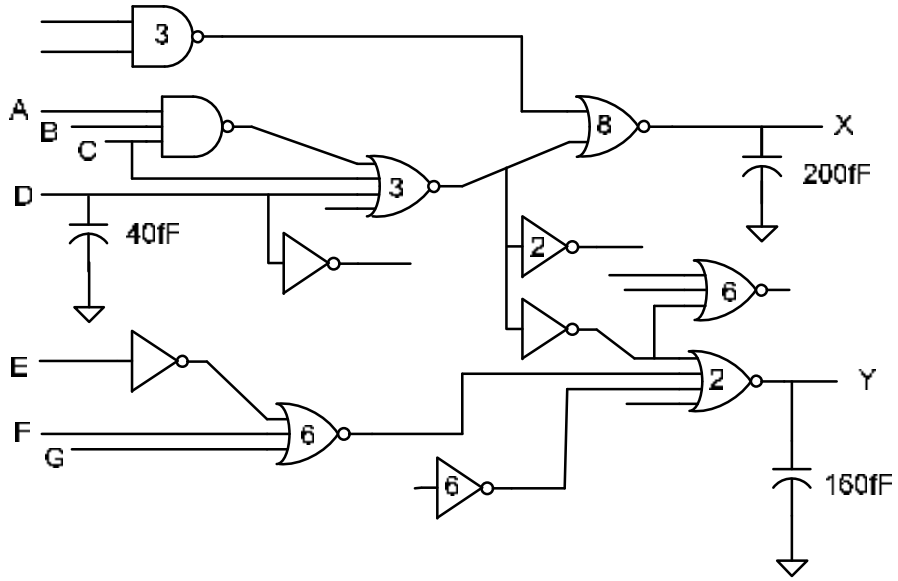
9. Describe the difference between ratiod logic and ratioless logic.

10. What is a binning model and what are the benefits and limitations of using a binning model?

Problem 1 A logic circuit designed in conventional static CMOS is shown. Assume all gates are sized for equal worst-case rise and fall times, that the input capacitance of an equal rise/equal fall reference inverter is 2fF, and that it has a propagation delay (T_{HL} + T_{LH}) of 20psec. The overdrive factor, if different than 1, is indicated by the number on the gate symbol.

a) Determine the propagation delay (T_{HL} + T_{LH}) from the D input to the Y output

b) Repeat part a) if the circuit is comprised entirely of minimum sized devices.



Problem 2 Assume the Nonlinear Device is characterized by the model equations

$$I_1 = 2V_1 + 4V_2^2$$
$$I_2 = 8V_1^3 + 0.25V_2$$

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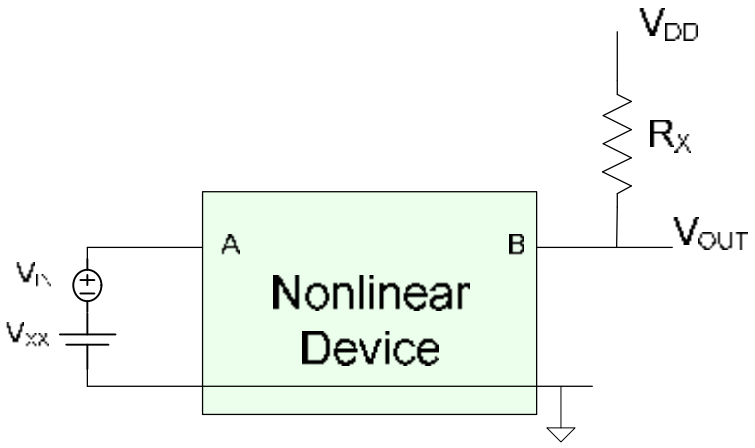
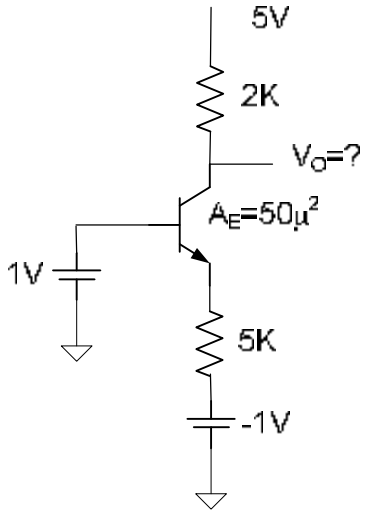
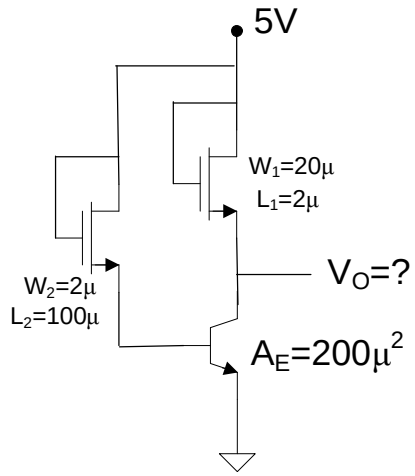
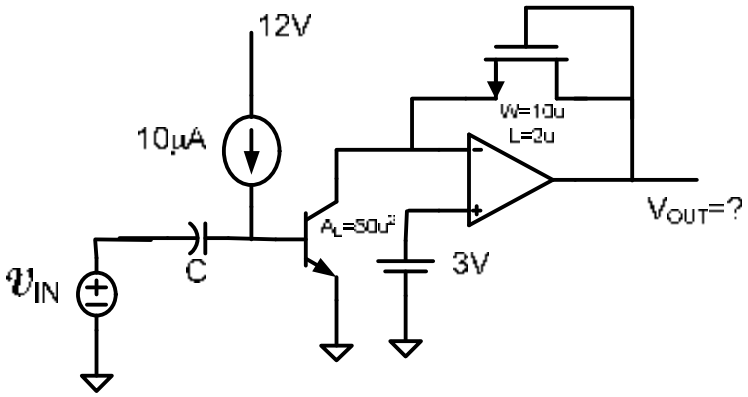
a) Obtain expressions for and draw a small-signal equivalent circuit of this nonlinear device at the Q-point defined by V_{1Q}=1V, V_{2Q}=2V.
b) (Extra Credit) Assume V_{IN} is a small-signal source. Obtain the quiescent output voltage and the small-signal voltage gain of the following circuit if V_{XX}=½V, V_{DD}=10V, and R_X= 4 Ω.



Problem 3 Determine the quiescent value of the output variable indicated with a ? If an excitation is shown, it is assumed to be a small-signal source.





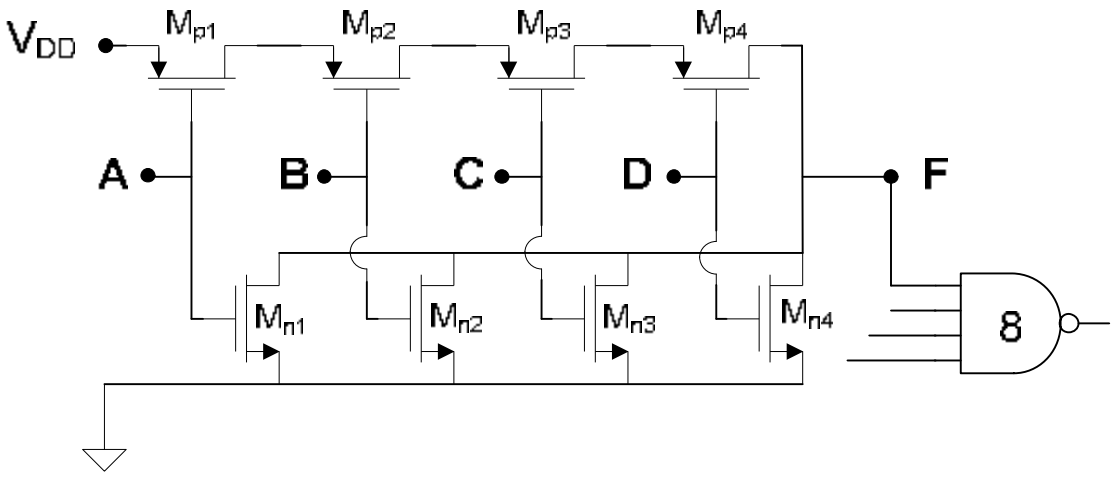


Problem 4

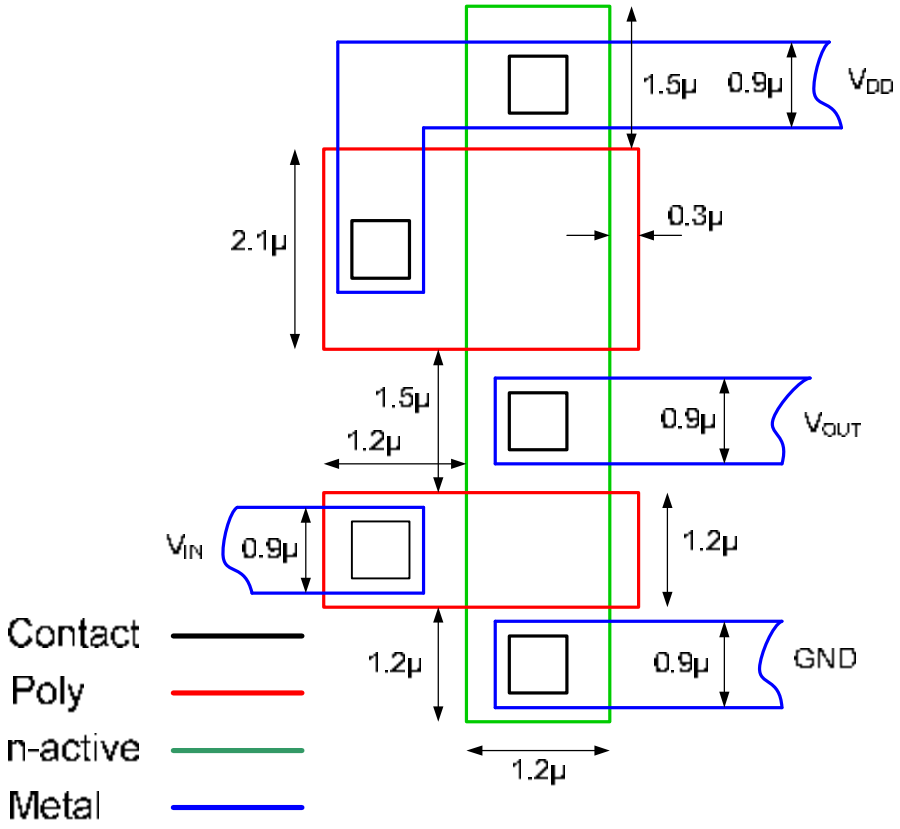
A 4-inut NOR gate is shown driving a 4-input NAND gate. Assume the NAND gate is sized for equal worst-case rise and fall times with an overdrive factor of 8 but a rather different sizing strategy was used for sizing the devices in the NOR gate. In the NOR gate, the four devices with either a "1" or "2" subscript were minimum-sized and those with either a "3" or "4" subscript were sized a if the entire NOR gate was to have equal worst-case rise and fall times with an overdrive factor of 4. Assume a minimum-sized equal rise/fall reference inverter in this process has an input capacitance of 4fF and the PD resistance of the reference inverter is 5K.

a) Determine the worst-case rise and fall times on the output F

b) What would they change to if all devices in the NOR gate were sized for equal worst-case rise and fall times with an overdrive factor of 4?



Problem 5 The layout of a circuit is shown along with 4 connections to the circuit labeled V_{IN}, V_{OUT}, GND and V_{DD}



a) Draw an equivalent circuit

b) If V_{DD}=5V, determine the value of V_{IN} required to obtain a quiescent output voltage of 2.5V

c) Give a high-frequency small-signal model for the lower transistor

TRANSISTOR PARAMETERS W/L N-CHANNEL P-CHANNEL UNITS

MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um